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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/658,981

09/10/2003

Dale John Shidla

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EXAMINER

ASSESSOR, BRIAN J

ART UNIT

PAPER NUMBER

2114

DATE MAILED: 05/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/658,981

Applicant(s)

SHIDLA ET AL.

Examiner

Brian J. Assessor

Art Unit

2114

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- ☒ Notice of References Cited (PTO-892)
- ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2/15/2005.
- ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- ☐ Notice of Informal Patent Application (PTO-152)
- ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 12 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 16 and 17 of copending Application No. 2005/0055683 A1. Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Claim 12 of the instant application contains every element of claims 16 and 17 of 2005/0055683 and thus anticipate the claim of the instant application. Claim 12 of the instant application therefore is not patentably distinct from the earlier patent claim and as such is unpatentable over obvious-type double patenting. A later application claim is

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not patentably distinct from an earlier claim if the later claim is not anticipated by the earlier claim.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 12-15 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. In claim 15 the program product needs to be stored on a computer readable medium in order to be acceptable under 35 USC 101. Claims 12-14 are "compiler" claims which are programs and are therefore non-statutory under 35 USC 101.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 5, 9-12, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fruehling (6,625,688) in view of Raina (6,134,675).

As per claim 1, Fruehling teaches:

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A method of compiling a program to be executed on a target microprocessor, the method comprising:

identifying a cycle during which a functional unit would otherwise be idle;

(Fruehling column 12, lines 60-65)

opportunistically scheduling a diagnostic operation for execution on the functional unit during that cycle; (Fruehling column 11, lines 32-34)

Fruehling fails to explicitly disclose a method for scheduling a comparison of a result from executing the diagnostic operation with a corresponding predetermined result.

In column 2, lines 7-13; Raina clearly discloses a method that compares the result of the processor being tested to an expected predetermined value. It would have been obvious to a person skilled in the art at the time of invention to include the comparison method as taught by Raina in order to create an effective testing method. This would have been obvious because Raina clearly teaches that the above process is better suited for creating a faster and improved processor testing method. (Raina column 1, lines 12-23)

As per claim 2:

The method of claim 1, further comprising:

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predetermining a test pattern of diagnostic operations and corresponding predetermined results for the functional unit. (Raina column 3, lines 19-21; there has been some test pattern developed in order to come up with the expected result.)

As per claim 5:

The method of claim 1, further comprising: setting a user-selectable level (‘slider’) for an aggressiveness of said opportunistic scheduling. (Fruehling column 12, lines 60-65; inherent; sliders are commonly used, allowing users to customize desired settings for any number of computer system operations.)

As per claim 9:

The method of claim 1, wherein the method is performed by a scheduler in a code generator of a program compiler. (Raina column 3, lines 7-11; the expected result is generated by the test device and then is compared to the processor values.)

As per claim 10:

The method of claim 9, wherein the program compiler comprises a native compiler for the target microprocessor. (Fruehling column 11, lines 58-65; the comparator is done within the target device.)

As per claim 11:

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The method of claim 9, wherein the program compiler comprises a cross compiler run on a different microprocessor. (Raina column 3, lines 7-11; the test is performed by an external testing device)

Claim 12 and 14 respectively are compiler claims corresponding to the method claims 1 and 2. Therefore claims 12 and 14 are rejected for the same rationale set forth in claims 1 and 2.

Claim 15 is a computer readable program claim corresponding to the method claim 1. Therefore claim 15 is rejected for the same rationale set forth in claim 1.

Claims 3, 4, 6-8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fruehling (6,626,688) in view of Raina (6,134,675) and in further in view of (Quach (6,640,313).

As per claim 3:

Fruehling and Raina fail to explicitly disclose a method, which causes a flag in the target microprocessor to be set when the comparison indicates an error.

In column 7, line 56 – column 6, line 2; Quach clearly discloses a method that uses flags to indicate when a test comparison has created an error. It would have been obvious to a person of normal skill in the art at the time of invention to include the method as taught by Quach in order to create a simple and effective method for indicating when an error in a test comparison has occurred. This would have been

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obvious because Quach clearly teaches that the above method is better suited for detecting errors in a processing environment, without creating more work for the processor. (Quach column 3, lines 22-25)

As per claim 4:

The method of claim 3, further comprising: if the error flag is set, then halting the execution and causing a notification to a user of the error flag. (Quach column 7, line 66 – column 6, line 8; there is an error signal created by the comparator when the results do not match)

As per claim 6:

Fruehling and Raina fail to explicitly disclose a method wherein the functional unit comprises a floating point unit.

In figure 1, element 158; Quach clearly discloses a method that tests functional units which comprise of floating point units. It would have been obvious to a person of normal skill in the art at the time of invention to include the method as taught by Quach in order to create a simple and effective method for testing processors through comparison. This would have been obvious because Quach clearly teaches that the above method is better suited for detecting errors in a processing environment, without creating more work for the processor. (Quach column 3, lines 22-25)

As per claim 7:

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Fruehling and Raina fail to explicitly disclose a method wherein the functional unit comprises an arithmetic logic unit.

In figure 1, element 154; Quach clearly discloses a method that tests functional units which comprise of arithmetic logic units. It would have been obvious to a person of normal skill in the art at the time of invention to include the method as taught by Quach in order to create a simple and effective method for testing processors through comparison. This would have been obvious because Quach clearly teaches that the above method is better suited for detecting errors in a processing environment, without creating more work for the processor. (Quach column 3, lines 22-25)

As per claim 8:

Fruehling and Raina fail to explicitly disclose a method wherein the functional unit comprises one of multiple functional units of a same type within the target microprocessor.

In column 6, lines 1-2; Quach clearly discloses a method that tests functional units which comprise of logic units of the same type. It would have been obvious to a person of normal skill in the art at the time of invention to include the method as taught by Quach in order to create a simple and effective method for testing processors through comparison. This would have been obvious because Quach clearly teaches that the above method is better suited for detecting errors in a processing environment, without creating more work for the processor. (Quach column 3, lines 22-25)

Claim 13 is a compiler claim corresponding to the method claim 8. Therefore claim 13 is rejected for the same rationale set forth in claim 8.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Assessor whose telephone number is (571) 272-0825. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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A handwritten signature in black ink, appearing to be 'SB', with a long horizontal flourish extending to the right.

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER